REMARKS

Claims 1-5 are pending. Claims 2 and 3 have been amended. New claim 6 has been added. No new matter has been introduced. Reexamination and reconsideration of the application are respectfully requested.

In the December 19, 2002 Office Action, the Examiner allowed claims 4 and 5. The Examiner rejected claim 1 under 35 U.S.C. §103(a) as being obvious over Fujimoto, U.S. Patent No. 5,473,348 (hereinafter '348 reference), taken with Matsumoto, U.S. Patent No. 5,929,839 (hereinafter '839 reference), in view of Tanaka et al., U.S. Patent No. 6,320,778 (hereinafter '778 reference). The Examiner objected to claims 2 and 3 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 2 and 3 have been amended, and new claim 6 has been added as per the Examiner's remarks. The §103(a) rejection is respectfully traversed.

The present invention relates to a display control apparatus that contains a video memory, a video memory controller, a color palette memory and a color palette replacer signal generator.

Independent claim 1 recites:

A display control apparatus comprising:

a video memory for storing color data, which are used to designate colors for displayed dots, palette data for use in conversion of the color data and address data representing addresses of the color data and the palette data;

a first video memory controller for reading the palette data from the video

memory in accordance with the address data, so that read palette data are written to a color palette memory;

a second video memory controller for reading the color data from the video memory in accordance with the address data, so that read color data are subjected to conversion on the color palette memory in accordance with the palette data; and

an output circuit for outputting either the color data read from the video memory or converted color data output from the color palette memory to a display,

wherein if present address data designating present palette data match with previous address data designating previous palette data, the first video memory controller does not write the present palette data to the color palette memory.

In the December 19, 2002 Office Action, the Examiner rejected claim 1 under 35 U.S.C. §103(a) as being obvious over Fujimoto, the '348 reference, taken with Matsumoto, the '839 reference, in view of Tanaka et al., the '778 reference.

The Examiner stated in the Office Action that Fujimoto teaches "a display control apparatus comprising: a video memory for storing color data, which are use to designate colors for displayed dots, palette data for use in conversion of the color data and address data representing addresses of the color data and the palette data (col. 7, lines 24-30)." The Examiner further stated "Fujimoto teaches a first video memory controller for reading the palette data from the video memory in accordance with address data, so that read palette data are written to a color palette memory (col. 7, lines 24-30)."

The '348 reference states "The color palette controller 390 performs color conversion of graphics data or text data. This controller 390 has built-in color two-stage

palette tables. The first color palette table consists of 16 color palette registers in each of which 6-bit color palette data is stored. The second color palette table consists of 256 color palette registers in each of which 18-bit color data, six bits for each of R, G and B, is stored." (col. 7, lines 24-30).

The '348 reference make no mention of a first video memory controller for reading the palette data from the video memory in accordance with address data, so that read palette data are written to a color palette memory. The '348 reference states the color palette controller 390 has built-in color two-stage palette tables. The first color palette table consists of 16 color palette registers in each of which 6-bit color palette data is stored. The second color palette table consists of 256 color palette registers in each of which 18-bit color data, six bits for each of R, G and B, is stored. The '348 reference does not state that the color palette controller 390 reads the palette data from the video memory in accordance with address data, so that read palette data are written to a color palette memory.

The '348 reference does state that "In graphics mode, memory data of 8 bits/pixel having the XGA specification is sent directly to the second color palette table without going through the first color palette table, and is converted into color consisting of 6 bits for each of R, G and B. Memory data of 4 bits/pixel having the VGA specification is sent first to the first color palette table by which it is converted into 6-bit color data. 2-bit data output from a built-in color select register is added to this 6-bit color data, yielding 8-bit color data. This 8-bit color data is then sent to the second color palette table by which it is converted into color data consisting of 6 bits for each of R, G and B." (col. 7, lines 31-41). However, memory data is in reference to data that is

converted to color data and not palette data used to carry out the conversion.

Therefore, '348 reference does not disclose, teach, or suggest a first video memory controller for reading the palette data from the video memory in accordance with address data, so that read palette data are written to a color palette memory as recited in independent claim 1.

Neither the Matsumoto '839 reference or the Tanaka '778 reference makes up for the shortcomings of the Fujimoto '348 reference.

Accordingly, applicant respectfully submits that independent claim 1 distinguishes over the above-cited reference. Claims 2 and 3 are rewritten in independent form and therefore are believed to be allowable as indicated in the Office Action. Claims 4 and 5 have been allowed.

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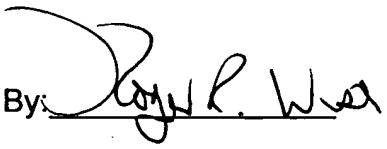
Applicant believes that the foregoing amendment and remarks place the application in condition for allowance, and a favorable action is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

PILLSBURY WINTHROP LLP

Date: April 21, 2003

By: 

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APPENDIX

VERSIONS WITH MARKINGS TO SHOW CHANGES MADE.

IN THE SPECIFICATION:

Please amend the paragraph on page 11 line 5 to line 8 as follows:

Namely, if the CPP31=0 and CPF=1 under the condition where the present CPP matches the previous CPP, the flow sequentially proceeds to steps S1, S3, S5, S6, and S2, in which the VRAM controller 12 does not proceed[s] to replacement of content of the color palette 13.

IN THE CLAIMS:

Please amend claims 2 and 3, and add new claim 6 as follows:

2. (Amended) [A display control apparatus according to claim 1] A display control apparatus comprising:

a video memory for storing color data, which are used to designate colors for displayed dots, palette data for use in conversion of the color data and address data representing addresses of the color data and the palette data;

a first video memory controller for reading the palette data from the video memory in accordance with the address data, so that read palette data are written to a color palette memory;

a second video memory controller for reading the color data from the video memory in accordance with the address data, so that read color data are subjected to conversion on the color palette memory in accordance with the palette data; and

an output circuit for outputting either the color data read from the video memory or converted color data output from the color palette memory to a display.

wherein at completion of writing the previous palette data to the color palette memory, the first video memory controller retains the previous address data designating the previous palette data in a register, so that the first video memory controller determines whether to replace content of the color palette memory by comparison between the present address data and the previous address data such that if present address data designating present palette data matches with previous address data designating previous palette data, the first video memory controller does not write the present palette data to the color palette memory.

3. (Amended) [A display control apparatus according to claim 1 or 2 wherein the video memory stores] A display control apparatus comprising:

a video memory for storing color data, which are used to designate colors for displayed dots, a color palette replacer instruction, [so that] palette data for use in conversion of the color data and address data representing addresses of the color data and the palette data;

a first video memory controller for reading the palette data from the video memory in accordance with the address data, so that read palette data are written to a color palette memory;

a second video memory controller for reading the color data from the video memory in accordance with the address data, so that read color data are subjected to conversion on the color palette memory in accordance with the palette data; and

an output circuit for outputting either the color data read from the video memory or converted color data output from the color palette memory to a display,

wherein if present address data designating present palette data match with

previous address data designating previous palette data, the first video memory controller does not write the present palette data to the color palette memory, if the color palette replacer instruction designates the color palette replacement, the first video memory controller proceeds to replacement of the content of the color palette memory unconditionally, regardless of the present or previous address data.

6. (New) A display control apparatus comprising:

a video memory for storing color data, which are used to designate colors for displayed dots, a color palette replacer instruction, palette data for use in conversion of the color data and address data representing addresses of the color data and the palette data;

a first video memory controller for reading the palette data from the video memory in accordance with the address data, so that read palette data are written to a color palette memory;

a second video memory controller for reading the color data from the video memory in accordance with the address data, so that read color data are subjected to conversion on the color palette memory in accordance with the palette data; and

an output circuit for outputting either the color data read from the video memory or converted color data output from the color palette memory to a display,

wherein at completion of writing the previous palette data to the color palette memory, the first video memory controller retains the previous address data designating the previous palette data in a register, so that the first video memory controller determines whether to replace content of the color palette memory by comparison between the present address data and the previous address data such that if present

address data designating present palette data match with previous address data designating previous palette data, the first video memory controller does not write the present palette data to the color palette memory, if the color palette replacer instruction designates the color palette replacement, the first video memory controller proceeds to replacement of the content of the color palette memory unconditionally, regardless of the present or previous address data.